IEEE Workshop on 'High Performance Digital Signal Processing System Design and Implementation' 15- 17 December 2015, Bhubaneswar, India.

(Put up on the request of IEEE Circuits & Systems (CAS) Society)

Venue: Samapnaturi Campus, IIT Bhubaneswar

An Outreach Activity of IEEE Circuits & Systems (CAS) Society

Coordinator: Dr. Pramod Meher, School of Computer Engineering, Nanyang Technological University, Singapore and Chapter Chair, IEEE Circuits & Systems Society Chapter, Singapore.

Motivation: Digital signal processing (DSP) is a ubiquitous technology which plays the central role in many different areas of applications, e.g., audio, video, image and speech processing, communications, medical instrumentation, automotive safety system, surveillance and target tracking operations, satellite and aerospace control, remote sensing, and many others. DSP algorithms are basically computation-intensive, and most of their applications are of real-time by nature. General purpose programmable systems very often do not meet the performance specification and area-constraint, but on the other hand, involve very high power consumption. DSP algorithms are required to be mapped to application specific architectures for implementation in ASIC and FPGA to meet the system level specifications. The objective of this workshop is to provide theoretical background and hands on training to the participants on the implementation of DSP algorithms in ASIC and FPGA along with an overview of advanced DSP applications.

Registration: Registration for this workshop is open to senior undergraduates, graduate students, and faculties. **Registration and participation is FREE of Charge. Interested students and faculties are invited to send the scan copy (or photograph) of signed and filled-in registration form in JPEG or PDF form to Dr. P. K. Meher at aspkmeher@ntu.edu.sg by 1st December 2015**. Highest preference will be given to members of IEEE Circuits & Systems Society and then to the IEEE Members and IEEE student members. Some free IEEE student membership and student membership of IEEE Circuits & Systems Society will be provided.

Tentative Program Outline

Day-1: 15-December 2015	
Time	**Event**
8.45 am to 9.15 am	Registration
9.15 am to 9.30 am	Welcome Address: by Dr. G. Panda, IIT Bhubaneswar
9.30 am to 10.30 am	Inaugural Keynote Address: by Dr. R.V. Raja Kumar, Director, IIT Bhubaneswar
10.30 am to 11.00 am	Tea and Networking
11.00 am to 12.30 pm	Talk-1: DSP Tools & Applications: by Dr. G. Panda, IIT Bhubaneswar
12.30 pm to 1.30 pm	Lunch
1.30 pm to 3.00 pm	Talk-2: Design Constraints & Design Space Exploration for Embedded DSP Systems: by Dr. P. K. Meher, Nanyang Technological University, Singapore
3.00 pm to 3.15 pm	Tea
3.15 pm to 5.15 pm	Lab Session-1: Introduction to HDL Coding and Synthesis Tools
Day-2: 16-December 2015	
Time	**Event**
9.15 am to 10.30 am	Keynote Address: Emerging Trends, Opportunities, and Challenges in Embedded Systems & IoT, by Dr. T. Srikanthan, Chair, School of Computer Engineering, Nanyang Technological University, Singapore
10.30 am to 11.00 am	Tea and Networking
11.00 am to 12.30 pm	Talk-3: Advanced DSP Systems: by Dr. G. Panda, IIT Bhubaneswar
12.30 pm to 1.30 pm	Lunch
1.30 pm to 3.00 pm	Talk-4: FPGA Devices and FPGA Implementation of Signal Processing Algorithms: by Dr. K. Sridharan, IIT Madras
3.00 pm to 3.15 pm	Tea
3.15 pm to 5.15 pm	Lab Session-2: Coding, Synthesis, and Testing for Fixed-Point Implementation of Basic Arithmetic Circuits
Day-3: 17-December 2015	
Time	**Event**
9.15 am to 9.30 am	Tea and Networking
9.30 am to 10.30 am	Talk-5: Image Processing Applications: by Dr. N. B. Puhan, IIT Bhubaneswar
10.30 am to 11.30 am	Talk-6: Graphical Representation of Algorithm and Transformations for Parallel Processing & Pipelining: by Dr. P. K. Meher, Nanyang Technological University, Singapore
11.30 am to 12.30 am	Talk-7: Typical DSP Algorithms and Their Complexity Considerations: by Dr. B. K. Mohanty, Jaypee University of Engineering and Technology, MP, India
12.30 pm to 1.30 pm	Lunch
1.30 pm to 3.30 pm	Lab Session-3: Coding and Synthesis of Parallel and Pipelined Circuits
3.30 pm to 3.45 pm	Tea
3.45 pm to 4.45 pm	Lab Session-4: Coding and Synthesis of Parallel and Pipelined Circuits
4.45 pm to 5.15 pm	Valediction and Distribution of Certificate

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Registration Form for Faculties

Full Name: _____

Designation:_____

Name of the Department/School :_____

Area of Specialization (if any) :_____

Name of the Institute:_____

IEEE Member : Yes ☐ No ☐

Member of IEEE Circuits and Systems Society: Yes ☐ No ☐

(If Yes) Membership No: _____

Address:_____

_____

City:_____ Postal Code:_____

Home Phone:_____ Mobile Phone Number: _____

Email:_____

Full Signature

Date:_____

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Registration Form for Students

Full Name: _____

Name of the Department/School :_____

Year of Study :_____

Name of the Institute:_____

IEEE Student Member : Yes ☐ No ☐

Student Member of IEEE Circuits and Systems Society: Yes ☐ No ☐

(If Yes) Membership No: _____

Address:_____

_____

City:_____ Postal Code:_____

Home Phone:_____ Mobile Phone Number: _____

Email:_____

Full Signature

Date:_____